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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re, Application of:

Fernando Gonzalez et al.

Serial No.: 10/751,141

Filed: December 31, 2003

For: Transistor Having Vertical Junction  
Edge and Method of Manufacturing  
the Same

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Group Art Unit: 2815

Examiner: Nguyen, Joseph H.

Atty. Docket: MICS:0114  
03-0027

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING  
37 C.F.R. 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:

November 12, 2004

Date

*Kerri Hyland*  
Kerri Hyland

**RESPONSE TO RESTRICTION REQUIREMENT**

In response to the Office Action (Restriction) mailed November 1, 2004, please amend  
the above-identified application as follows: